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ABSTRACT:

CHG DATE=19990617 STATUS=O> This invention provides an E/D integrated circuit
obtained by connecting an enhancement transistor (Q2) serving as a switching
transistor to a depletion transistor (Q1) serving as a load and having a gate
length (Lg1) larger than a gate length (Lg2) of the enhancement transistor in
series with each other. <IMAGE>

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(54) E/D integrated circuit formed in compound semiconductor substrate.

(57) This invention provides an E/D integrated circuit obtained by connecting an enhancement transistor (Q2) serving as a switching transistor to a depletion transistor (Q1) serving as a load and having a gate length (Lg1) larger than a gate length (Lg2) of the enhancement transistor in series with each other.

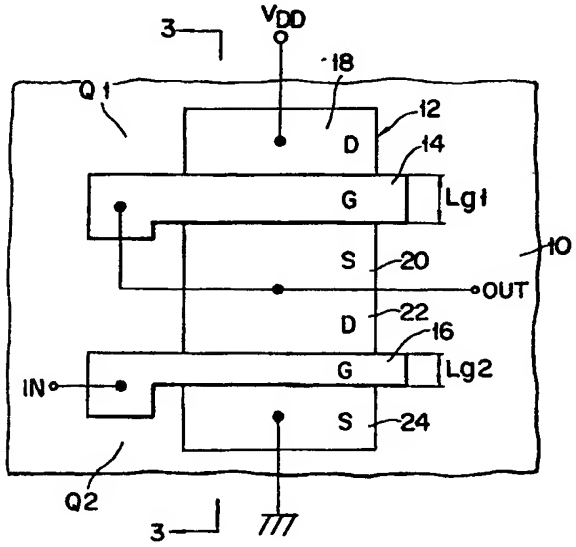

FIG. 2

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E/D INTEGRATED CIRCUIT FORMED IN COMPOUND SEMICONDUCTOR SUBSTRATE

The present invention relates to an E/D integrated circuit obtained by connecting a depletion field effect transistor serving as a load and an enhancement field effect transistor serving as a switching transistor in series with each other and, more particularly, to an improvement of the performance of the E/D integrated circuit when it is formed in a compound semiconductor substrate.

As an E/D circuit obtained by connecting a depletion field effect transistor (to be referred to as a D-type FET or a D-type MESFET hereinafter) serving as a load and an enhancement field effect transistor (to be referred to as an E-type FET or an E-type MESFET hereinafter) serving as a switching transistor in series with each other, an E/D inverter is widely known.

In a conventional method, in order to add a parasitic capacitance to an E/D inverter or the like, a gate length and a gate width generally have minimum dimensions. This is a condition which is necessarily required for an E-type FET serving as a switching transistor requiring a high-speed operation. In a D-type FET serving as a load, this condition is satisfied. Therefore, the gate lengths of the D-type FET serving as a load and the E-type FET serving as a switching transistor are equal to each other.

However, in minimum dimensions, i.e., in a range of a gate length obtained by the most advanced process, a threshold voltage of an FET largely varies. This case is shown in Fig. 1. Fig. 1 is a view schematically showing a relationship between the gate length and threshold voltage of a transistor. As shown in Fig. 1, in a range r of a gate length obtained by the most advanced process, a threshold value largely varies due to small process fluctuations. Especially in an E/D inverter, when the threshold voltage of a D-type FET serving as a load varies, a current supplied to an E-type FET serving as a switching transistor connected in series with the D-type FET varies. When a current supplied to the E-type FET varies, a variation in output voltage or the like is caused, and the performance serving as the switching circuit is degraded. Since a process technique is not sufficiently established especially in a GaAs IC/LSI, a variation in threshold value of the GaAs IC/LSI due to process fluctuations is larger than that of a silicon IC/LSI. For this reason, in the GaAs IC/LSI, a circuit design capable of absorbing the process fluctuation is desired.

The present invention has been made in consideration of the above problem, and has as its object to provide an E/D integrated circuit for obtaining a circuit design capable of absorbing process fluctuations and of obtaining excellent performance even when the E/D integrated circuit is formed in a compound semiconductor substrate.

The above object can be achieved by the following arrangement.

According to the present invention, an integrated circuit is obtained by connecting an E-type FET serving as a switching transistor and a D-type transistor serving as a load and having a gate length larger than that of the E-type FET in series with each other.

In the above integrated circuit, the gate length of the D-type FET serving as a load is set to be larger than the gate length of the E-type FET serving as a switching transistor. For example, the gate length of the E-type FET is formed to have a minimum dimension obtained by the most advanced process, the gate length of the D-type FET is larger than the gate length having the minimum dimension of the E-type FET. Therefore, even when process fluctuations occur, the gate length is formed to have a dimension falling within a range wherein a threshold value is stable. Therefore, a variation in threshold voltage of the D-type FET serving as a load is prevented, a stable current can be constantly supplied to the E-type FET serving as a switching transistor, and an output from the circuit is stabilized.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a graph showing a relationship between a gate length and a threshold value;

Fig. 2 is a plan view showing a pattern of an integrated circuit according to the first embodiment of the present invention;

Fig. 3 is a sectional view showing the integrated circuit along a line 3 - 3 in Fig. 2;

Fig. 4 is an equivalent circuit diagram showing the integrated circuit shown in Figs. 2 and 3;

Fig. 5 is a plan view showing a pattern of an integrated circuit according to the second embodiment of the present invention;

Fig. 6 is a sectional view showing the integrated circuit along a line 6 - 6 in Fig. 5;

Fig. 7 is a plan view showing a pattern of an integrated circuit according to the third embodiment of the present invention;

Fig. 8 is a sectional view showing the integrated circuit along a line 8 - 8 in Fig. 7;

Fig. 9 is an equivalent circuit diagram showing the integrated circuit shown in Figs. 7 and 8;

Fig. 10 is a plan view showing a pattern of an integrated circuit according to the fourth embodiment of

the present invention;

Fig. 11 is a sectional view showing the integrated circuit along a line 11 - 11 in Fig. 10;

Fig. 12 is a sectional view showing the integrated circuit along a line 12 - 12 in Fig. 11; and

Fig. 13 is an equivalent circuit diagram showing the integrated circuit shown in Figs. 10 to 12.

Embodiments of the present invention will be described below with reference to the accompanying drawings.

[First Embodiment]

Fig. 2 is a plan view showing a pattern of an integrated circuit according to the first embodiment of the present invention. This view illustrates an E/D inverter of a DCFL (Direct Coupled FET Logic) circuit as an example. Fig. 3 is a sectional view showing the E/D inverter along a line 3 - 3 in Fig. 2, and Fig. 4 is an equivalent circuit diagram of the E/D inverter.

As shown in Figs. 2 to 4, an active region 12 for constituting a source/drain or a channel is formed in a surface region of a GaAs substrate 10. A gate electrode 14 of a D-type MESFET Q1 and a gate electrode 16 of an E-type MESFET Q2 are formed in the active region 12. A drain 18 of the D-type MESFET Q1 is connected to a high-potential power source VDD. A source 20 of the D-type MESFET Q1 is integrated with a drain 22 of the E-type MESFET Q2. A source 24 of the E-type MESFET Q2 is connected to a low-potential power source, e.g. ground. An input terminal IN is connected to the gate electrode 16 of the E-type MESFET Q2 serving as a switching transistor. An output terminal OUT is connected to the source region 22 of the the E-type MESFET Q1 and to the drain region 22 of the E-type MESFET Q2 and connected to the gate electrode 14 of the D-type MESFET Q1.

The DCFL circuit with the above arrangement is operated as an inverter, as is apparent from an equivalent circuit diagram in Fig. 4.

According to the present invention, a gate length Lg1 of the D-type MESFET Q1 serving as a load is set to be larger than a gate length Lg2 of the E-type MESFET Q2 serving as a switching transistor. In the above DCFL circuit, in order to maximize high-speed performance, the gates of the D-type MESFET Q1 and of the E-type MESFET Q2 are formed by the most advanced process. The formation using the most advanced process means that the gate length of the gate electrode is set to be a minimum dimension obtained by a state-of-the art technique. In this case, an influence of the threshold voltage of the MESFET for the gate length is schematically shown in Fig. 1. In Fig. 1, the gate length obtained by the most advanced process is plotted in a hatched portion where the threshold voltage begins to fall from a constant value, i.e., a region $\bar{r}$ in Fig. 1.

In an individual unit process or a silicon device made of a stable substrate material, since the gate length obtained by the most advanced process can be controlled with good reproducibility and high accuracy, variations in threshold voltage of MESFETs are small. However, in a compound semiconductor device represented by a GaAs device, an unit process is technically inferior to that of a silicon device, and the substrate made of two types of materials is not stable compared with a substrate made of silicon or the like. Therefore, the gate length cannot be controlled by the most advanced process with good reproducibility and high accuracy. As a result, the MESFETs have large variations in threshold voltage. In the compound semiconductor device, since the unit process and the substrate are less stable than the silicon device, the gate length is difficult to be controlled by the most advanced process.

In the E/D inverter shown in the equivalent circuit diagram of Fig. 4, a maximum operating speed of an E-type MESFET Q2 serving as a switching transistor must be obtained. For this reason, the E-type MESFET Q2 must have a gate length having a minimum dimension obtained by the most advanced process, i.e., a gate length falling within a range $\bar{r}$ in Fig. 1.

The D-type MESFET Q1 is used for supplying a current $\bar{i}$ to the E-type MESFET Q2. The present invention is made in consideration of stably supplying the current $\bar{i}$ to the E-type MESFET Q2, and a gate length larger than the gate length having a minimum dimension falling within the range $\bar{r}$ in Fig. 1 is employed to the D-type MESFET Q1 serving as a load. That is, the gate length falls outside the range $\bar{r}$ in Fig. 1, and the threshold voltage of the MESFET is to be stable even when process fluctuations occur. Therefore, the D-type MESFET Q1 can always supply the constant current $\bar{i}$ to the E-type MESFET Q2 serving as a switching transistor.

In a GaAs digital IC/LSI, in order to stably obtain the above effect, assuming that the gate length Lg2 of the E-type MESFET serving as a switching transistor has a minimum dimension obtained by the most advanced process, the gate length Lg1 of the D-type MESFET Q1 serving as a load desirably satisfies the following condition.

$$Lg1 \geq 1.5 \times Lg2 \quad (1)$$

As shown in equation (1), when the gate length Lg1 of the D-type MESFET Q1 serving as a load is set to be 1.5 times or more the gate length Lg2 of the E-type MESFET Q2 serving as a switching transistor, the threshold voltage of the MESFET is sufficiently stable even when process fluctuations occur.

In an E/D inverter according to the first embodiment, the length Lg1 of the D-type MESFET Q1 serving as a load is set to be a length which allows the threshold voltage to be stable even when process fluctuations occur. Therefore, a stable current can be supplied to the D-type MESFET Q2 serving as a switching transistor, and a voltage output from the output terminal OUT can be stabilized. In addition, since the gate length Lg2 of the E-type MESFET Q2 is set to be a minimum gate length obtained by the most advanced process, a parasitic capacitance is decreased to increase a switching speed.

[Second Embodiment]

In a MESFET having a large gate length, a drain current tends to be decreased. In the integrated circuit according to the first embodiment, the D-type MESFET Q1 has this tendency. In order to keep a current which can be supplied from the E-type MESFET Q2 having a gate length of a minimum dimension to be equal to a current which can be supplied from the D-type MESFET Q1 serving as a load at the same value, the gate width of the E-type MESFET Q2 is set to be smaller than the gate width of the D-type MESFET Q1.

Fig. 5 is a plan view showing a pattern of an inverter designed on the basis of the above idea, and Fig. 6 is a sectional view showing the inverter along a line 6 - 6 in Fig. 5. The same reference numerals as in Figs. 2 and 3 denote the same parts in Figs. 5 and 6.

As shown in Fig. 5, a gate width Wg2 of the E-type MESFET Q2 is set to be smaller than a gate width Wg1 of the D-type MESFET Q1. In this case, a current which can be supplied from the D-type MESFET Q1 can be equal to a current which can be supplied from the E-type MESFET Q2, and the performance of the E-type MESFET Q2 can be maximized.

To make a current which can be supplied from the D-type MESFET Q1, equal to a current which can be supplied from the E-type MESFET Q2, as described above, it is desirable that the gate widths Wg1 and Wg2 satisfy the following condition.

A drain current I_D of an FET is schematically expressed by:

$$I_D = \frac{W}{\cdot} \cdot \mu \cdot C\{(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\} \quad (2)$$

where μ: carrier mobility, V_{GS}: gate-source voltage, C: capacitance, V_{DS}: drain-source voltage, V_{th}: threshold voltage of FET

Therefore, a drain current I_{D1} of the MESFET Q1 can be expressed by the following equation:

$$I_{D1} = \frac{Wg1}{Lg1} \cdot \mu \cdot C\{(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\} \quad \cdots (3)$$

Similarly, a drain current I_{D2} of the MESFET Q2 is expressed by the following equation:

$$I_{D2} = \frac{Wg2}{Lg2} \cdot \mu \cdot C\{(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\} \quad \cdots (4)$$

Since the MESFET Q1 and the MESFET Q2 are formed and integrated in the same substrate, it can be assumed that terms of $\mu \cdot C\{(V_{GS} - V_{th})V_{DS} - (1/2)V_{DS}^2\}$ of equations (3) and (4) have substantiality equal values. Therefore, the currents I_{D1} and I_{D2} can be expressed by the following equation:

$$\frac{Wg1}{Lg1} = \frac{Wg2}{Lg2} \quad \cdots (5)$$

According to equation (5), in order to make the currents I_{D1} and I_{D2} to have the same value, the gate widths Wg1 and Wg2 satisfy the following equation:

$$Wg2 = \frac{Lg2}{Lg1} \cdot Wg1 \quad \ldots (6)$$

In designing the circuit, the gate widths Wg1 and Wg2 are set to the optimal values which are determined by other various design and structural factors. Therefore, the optimal values are not necessarily be those values shown in Fig. 5, or need not satisfy equation (6).

[Third Embodiment]

According to the third embodiment, the present invention is applied to an E/D NAND circuit of a DCFL circuit. Fig. 7 is a plan view showing a pattern of the E/D NAND, Fig. 8 is a sectional view showing the E/D NAND circuit along a line 8 - 8 in Fig. 7, and Fig. 9 is an equivalent circuit diagram thereof.

As shown in Figs. 7 to 9, a drain 18 of a D-type MESFET Q3 serving as a load is connected to a high-potential power source VDD, and a source 20 of the D-type MESFET Q3 is connected to a gate electrode 14 and an output terminal OUT. E-type MESFETs Q4 and Q5 serving as switching transistors are connected between the source 20 of the D-type MESFET Q3 and a low-potential power source, e.g., ground, in series with each other. A drain 22A of the E-type MESFET Q4 is formed integrally with the source 20 of the D-type MESFET Q5, and the source 24A of the E-type MESFET Q4 is formed integrally with a drain 22B of the E-type MESFET Q5. A source 24B of the E-type MESFET Q5 is connected to, e.g., ground. Input terminals IN1 and IN2 are connected to the gates of the E-type MESFETs Q4 and Q5, respectively.

In the E/D HAND circuit with the above arrangement, as in the first embodiment, a gate length larger than a gate length obtained by the most advanced process is employed as the gate length Lg1 of the D-type MESFET serving as a load such that the threshold voltage is stable even when process fluctuations occur.

As the gate lengths Lg2 of the E-type MESFETs Q4 and Q5 serving as switching transistors, gate lengths obtained by the most advanced process are employed to increase a switching speed.

As in the second embodiment, although not shown, the gate widths of the E-type MESFETs Q4 and Q5 may be smaller than the gate width of the D-type MESFET Q3, and currents which can be supplied from the E-type MESFETs Q4 and Q5 may be equal to a current which can supplied from the D-type MESFET Q3.

[Fourth Embodiment]

According to the fourth embodiment, the present invention is applied to an E/D NOR circuit of a DCFL circuit. Fig. 10 is a plan view showing a pattern of the E/D NOR circuit, Fig. 11 is a sectional view showing the E/D NOR circuit along a line 11 - 11 in Fig. 10, Fig. 12 is a sectional view showing the E/D NOR circuit along a line 12 - 12 in Fig. 10, and Fig. 13 is an equivalent circuit diagram thereof.

As shown in Figs. 10 to 13, a drain 18 of a D-type MESFET Q6 serving as a load is connected to a high-potential power source VDD, and a source 20 of the D-type MESFET Q6 is connected to a gate electrode 14 and an output terminal OUT. E-type MESFETs Q7 and Q8 are parallelly connected between a source 20 of the D-type MESFET Q6 and a low-potential power source such as ground. Drains 22C and 22D of the E-type MESFETs Q7 and Q8 are formed integrally with the source 20 of the D-type MESFET Q6. Sources 24C and 24D of the E-type MESFETs Q7 and Q8 are formed integrally with each other and connected to, e.g., ground. Input terminals IN1 and IN2 are connected to the gates of the E-type MESFETs Q7 and Q8, respectively.

In the E/D NOR circuit with the above arrangement, as in the first embodiment, the gate length Lg1 of the D-type MESFET Q6 serving as a load is a gate length which is stable even when process fluctuations occur.

Gate lengths Lg2 of the E-type MESFETs Q7 and Q8 serving as switching transistors are minimum gate lengths obtained by the most advanced process.

As in the second embodiment, the gate lengths of the E-type MESFETs Q7 and Q8 may be smaller than the gate width of the D-type MESFET Q6, and currents which are supplied from the D-type and E-type MESFETs may be equal to each other.

The DCFL circuits explained in the first to fourth embodiments have a high speed operation and can

provide a stable output. Since the threshold voltage of the D-type MESFET serving as a load slightly varies even when process fluctuations occur in the production, variations and fluctuations in output value of the circuit are hard to occur.

An increase in parasitic capacitance due to increases in gate length and gate width of the D-type MESFET serving as a load rarely influences the switching speed of the circuit because the D-type MESFET connected to a gate and source supplies a current up to a current saturation region in advance.

The present invention is preferably applied to a compound semiconductor device (compound semiconductor digital IC/LSI) manufactured by a developing process technique. However, the present invention is not limited to the compound semiconductor device. When it can be applied to a semiconductor device such as a silicon device consisting of a one-element material, the same effect as described above can be obtained.

Claims

1. An integrated circuit comprising an enhancement transistor serving as a switching transistor and a depletion transistor serving as a load and connected in series with said enhancement transistor, characterized in that
a gate length of said depletion transistor serving as a load is larger than a gate length of said enhancement transistor.

2. An integrated circuit according to claim 1, characterized in that a gate width of said enhancement transistor is smaller than a gate width of said depletion transistor serving as a load.

3. An integrated circuit according to claims 1 and 2, characterized in that the gate length of said depletion transistor is not less than 1.5 times the gate length of said enhancement transistor.

4. An integrated circuit according to claim 2, characterized in that when the gate length and the ate width of said depletion transistor are represented by and Wg1 and the gate length and the gate width of said enhancement transistor are represented by Lg2 and Wg2, the following equation is satisfied:

$$Wg2 = \frac{Lg2}{Lg1} \cdot Wg1$$

5. An integrated circuit according to claim 1, characterized in that said depletion transistor and said enhancement transistor are MESFETs.

6. An integrated circuit according to claim 5, characterized in that said MESFETs are formed in a compound semiconductor substrate.

7. An integrated circuit according to claim 6, characterized in that said compound semiconductor substrate is made of GaAs.

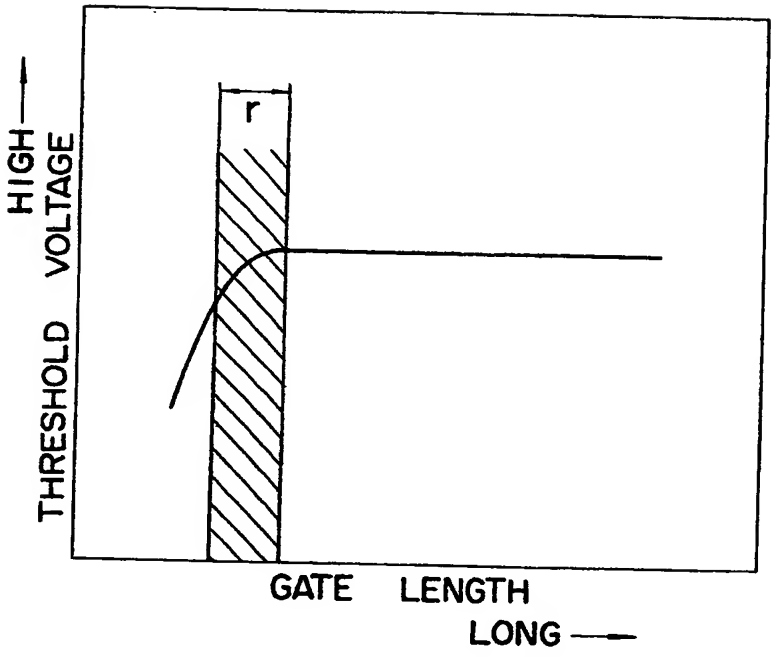

FIG. 1

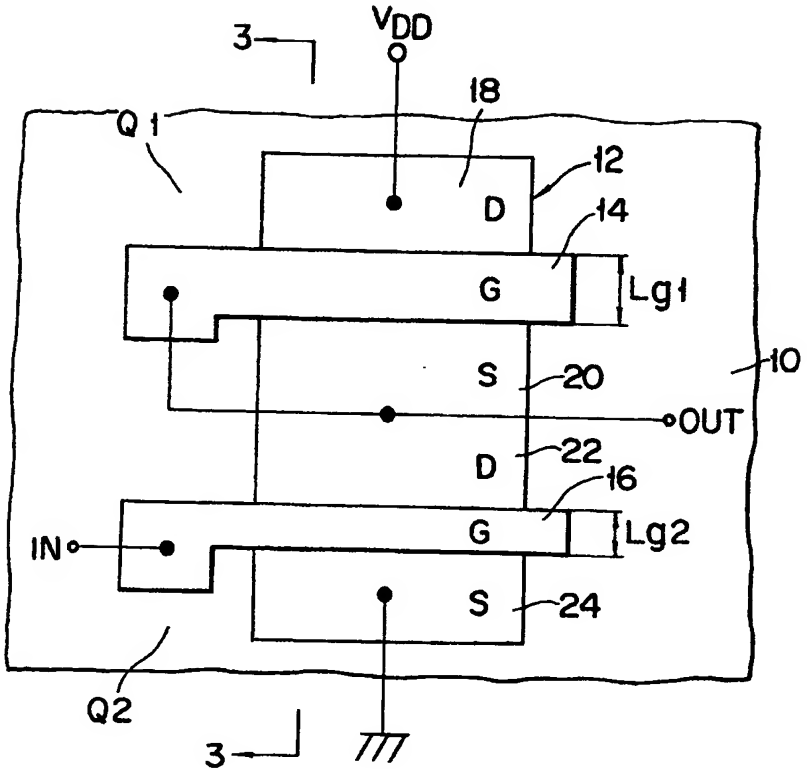

FIG. 2

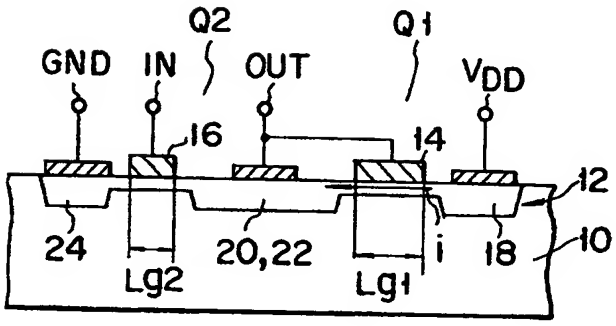

FIG. 3

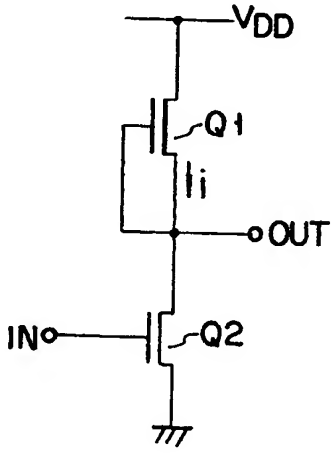

FIG. 4

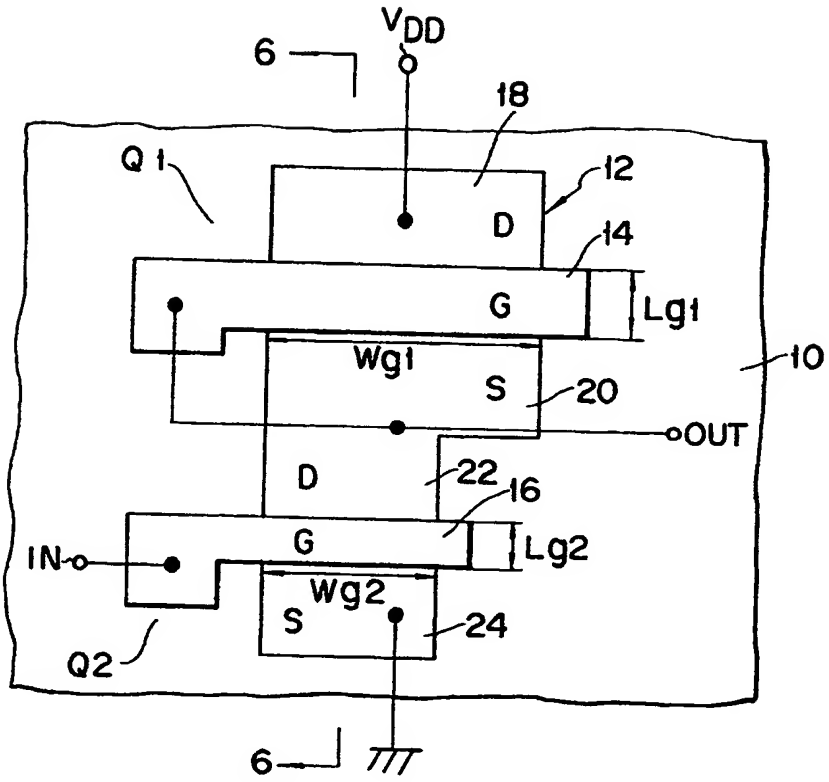
VDD
6
18
Q1
12
D
14
G
Lg1
Wg1
S
20
10
OUT
D
22
16
G
Lg2
IN
Wg2
S
24
Q2
6

FIG. 5

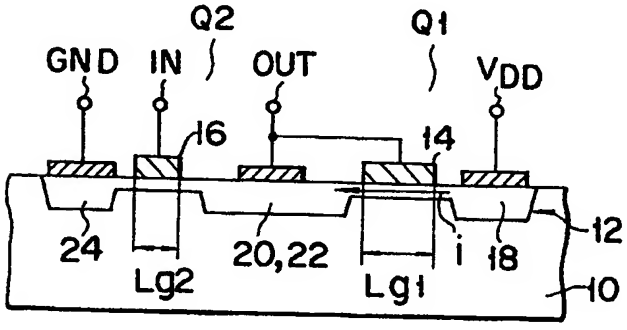
Q2
Q1
GND
IN
OUT
VDD
16
14
24
20,22
i
18
12
Lg2
Lg1
10

FIG. 6

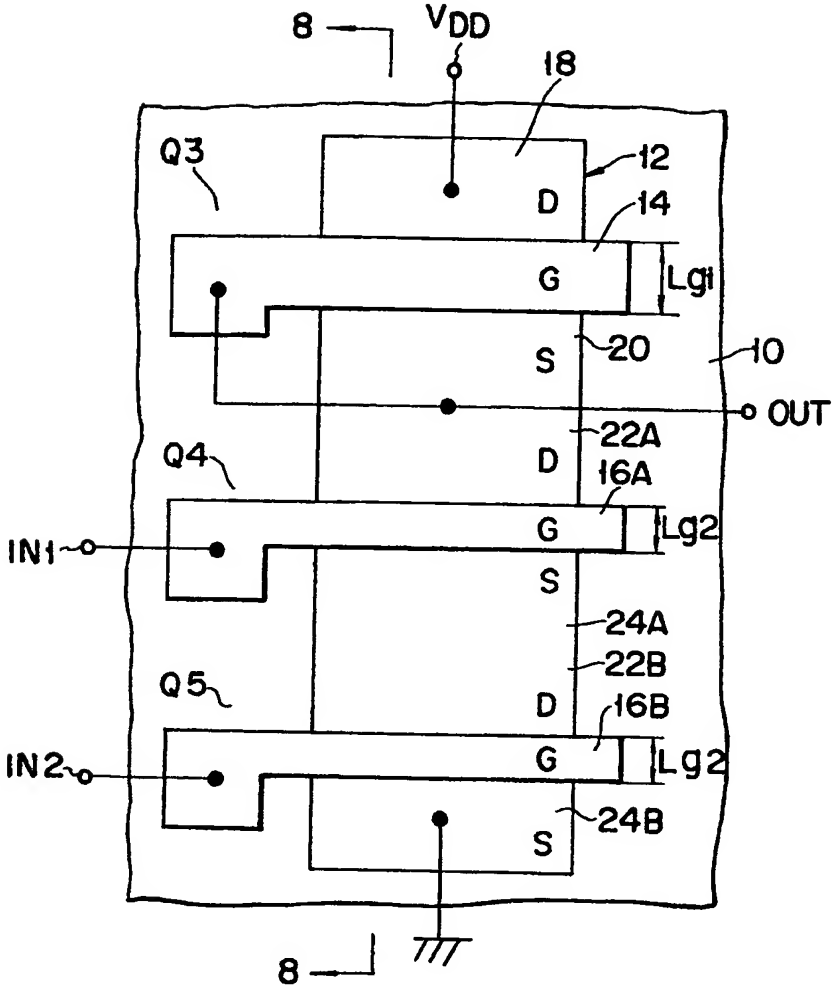
8
VDD
18
Q3
12
D
14
G
Lg1
S
20
10
OUT
22A
Q4
D
16A
G
Lg2
IN1
S
24A
22B
Q5
D
16B
G
Lg2
IN2
24B
S
8

FIG. 7

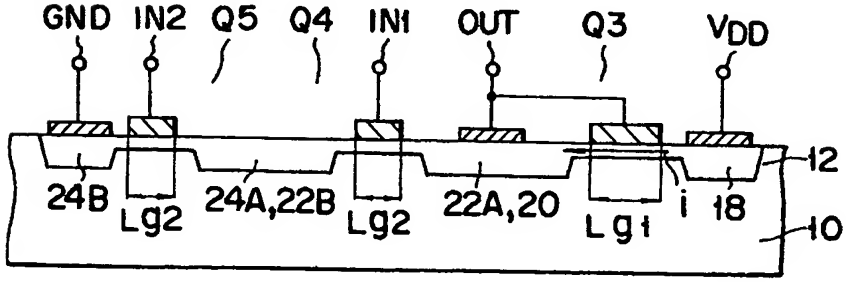
GND
IN2
Q5
Q4
IN1
OUT
Q3
VDD
12
24B
Lg2
24A,22B
Lg2
22A,20
Lg1
i
18
10

FIG. 8

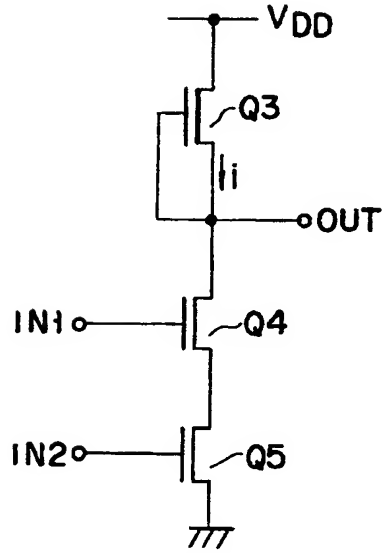
VDD
Q3
i
OUT
IN1
Q4
IN2
Q5

FIG. 9

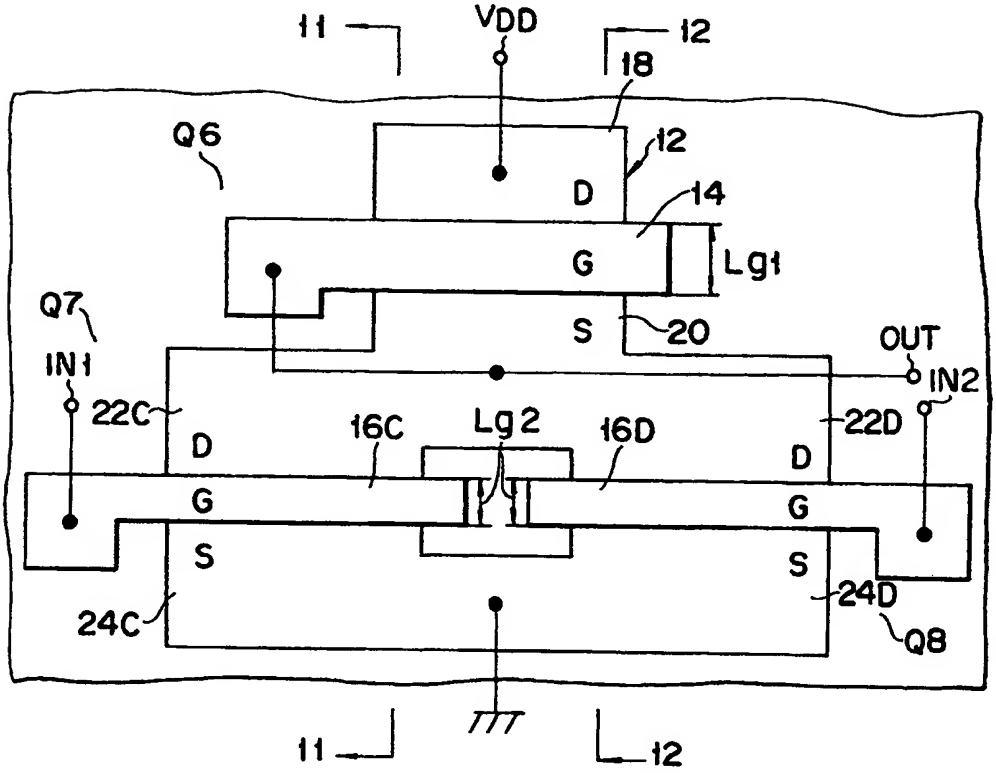
11
VDD
12
18
Q6
12
D
14
G
Lg1
Q7
S
20
OUT
IN1
IN2
22C
16C
Lg2
16D
22D
D
D
G
G
S
S
24C
24D
Q8
11
12

FIG. 10

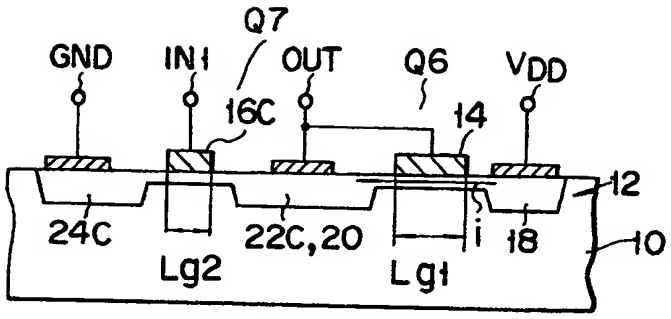

FIG. 11

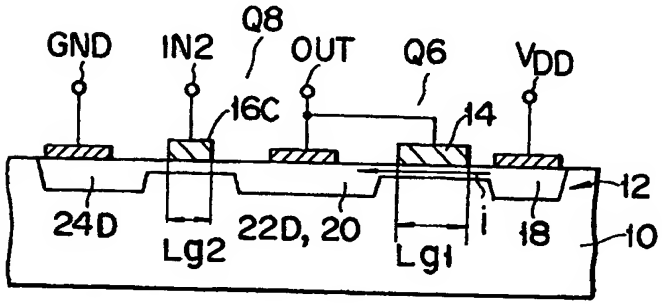

FIG. 12

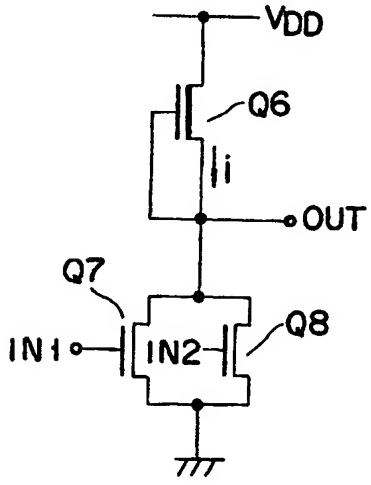

FIG. 13